IN THE SPECIFICATION

The paragraph beginning at page 4, line ~~10~~ 8 is amended as follows

Figs. 1A - 1C contain illustrations of how pulse width modulation can be used to control power to a load such as, for example, an LED or array of LEDs. The PWM duty cycle is the ratio of the amount of time the pulse is on, ~~to the interval of time in which the pulse is off~~ to the total period of the cycle. In the example of Fig. 1A, a pulse 2 is on during the interval from t=0 seconds to t=0.25 milliseconds (*ms*). No pulse occurs for the interval from t=0.25*ms* to t=1*ms* for a total of 0.75*ms*. The duty cycle in the example of Fig. 1A is therefore 1/4. The duty cycle in the example of Fig. 1B is 1/2, and the duty cycle of Fig. 1C is 3/4.

The paragraph beginning on page 8, ending on page 9, line 4 on page 9 is amended as follows:

For example, suppose the example two bit modulator of Table I was required to have increased resolution according to the techniques of the present invention while maintaining an update rate of at least 100 Hz. A virtual five bit pulse width modulator with an update speed of 125 Hz could be created by adding additional timer states as shown in Table II. A total of 8 states are required, which for an additional timer period of 1*ms* yields an 8*ms* total period. The resulting minimum duty cycle is thus $1/2^5$, or 1/32. This modulation scheme is shown in Fig. 5A. However, increasing the virtual modulation to six bits equates to a minimum duty cycle of $1/2^6$ or 1/64. For the two bit modulator of Table I, and per Table II, 16 timer states are required for a total time period of 16*ms*. The resulting ~~waveform~~ modulation scheme is as shown in Fig. 5B. The update rate is thus 62.5 Hz which does not meet the 100 Hz update requirements specified for the system.

The paragraph beginning on page 10, line 3 is amended as follows:

Fig. 8 contains a flow chart of a process useful for implementing the improved pulse width modulation of the present invention. In the flow chart of Fig. 8, the desired duty cycle is specified in step 700 as a word having [[n =]] $\underline{n = n +} \log_2 K$ significant bits. In steps 702 and 704, the word is truncated to the maximum number permitted if the word received is in excess of this value. In step 706, the current state of the additional timer is determined. The various steps shown grouped together by braces 708 of Fig. 8 assign a modulator output value to the given timer state. In a preferred embodiment of the invention, the modulator outputs associated with each of the various states are within one of the other. Other combinations are possible, however, in a preferred embodiment of the invention, steps 710 and 712 are used to ensure that a valid modulator output is specified at start up; and in conjunction with step 709, are used to validate that the modulator output specified is within the maximum and minimum values expected for this state. Step 714 checks if a 100% duty cycle is needed for this state and if so, step 716 asserts the modulator overflow bit. Otherwise, the desired modulator output value is set in step 718 and the overflow bit deasserted in step 720. The modulator output for the current state is now established. Step 722 increments to the next state and the modulator output for that state is set by repeating the process flow of Fig. 8.